

1/2-Inch 3-Megapixel CMOS Digital Image Sensor

MT9T001P12STC

For the latest data sheet, refer to Aptina's Web site: www.aplina.com

Features

- High frame rate
- Global reset release
- Horizontal and vertical binning
- Column and row skip modes
- Superior low-light performance
- Low dark current
- Simple two-wire serial interface
- Programmable controls: Gain, frame rate, frame size, exposure
- Pin-for-pin compatible with Aptina's 1.3-megapixel MT9M001 and 2-megapixel MT9D001

Applications

- Digital still cameras
- Digital video cameras
- Converged DSCs/camcorders

General Description

The Aptina[®] MT9T001 is a QXGA-format 1/2-inch CMOS active-pixel digital image sensor with an active imaging pixel array of 2,048H x 1,536V. It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface.

The 3-megapixel CMOS image sensor features Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a QXGA image at 12 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical format		1/2-inch (4:3)
Active imager size		6.55mm(H) x 4.92mm(V) 8.19 (Diagonal)
Active pixels		2,048H x 1,536V
Pixel size		3.2 μ m x 3.2 μ m
Color filter array		RGB Bayer pattern
Shutter type		Global reset release (GRR), electronic rolling shutter (ERS)
Maximum data rate/ master clock		48 MPS/48 MHz
Frame rate	QXGA (2,048 x 1,536)	Programmable up to 12 fps
	UXGA (1,600 x 1,200)	Programmable up to 20 fps
	SXGA (1,280 x 1,024)	Programmable up to 27 fps
	XGA (1,024 x 768)	Programmable up to 43 fps
	VGA (640 x 480)	Programmable up to 93 fps
ADC resolution		10-bit, on-chip
Responsivity		>1.0 V/lux-sec (550nm)
Dynamic range		61dB
SNR _{MAX}		43dB
Supply voltage		3.0V–3.6V (3.3V nominal)
Power consumption		240mW (nominal); 2?W (standby)
Operating temperature		0°C to +60°C
Packaging		48-pin PLCC

The MT9T001 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and industrial applications, including digital still cameras, digital video cameras, and PC cameras.

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General Description (continued)

Figure 1: Block Diagram

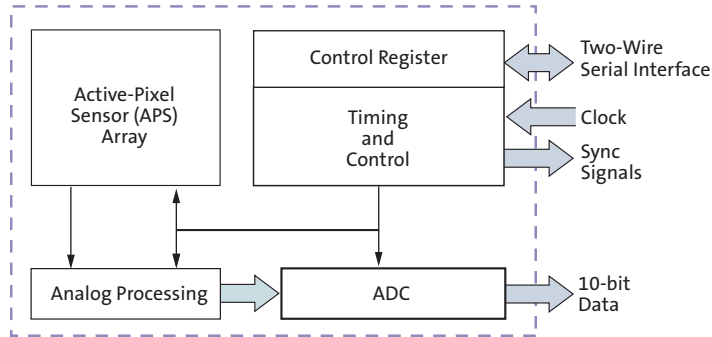
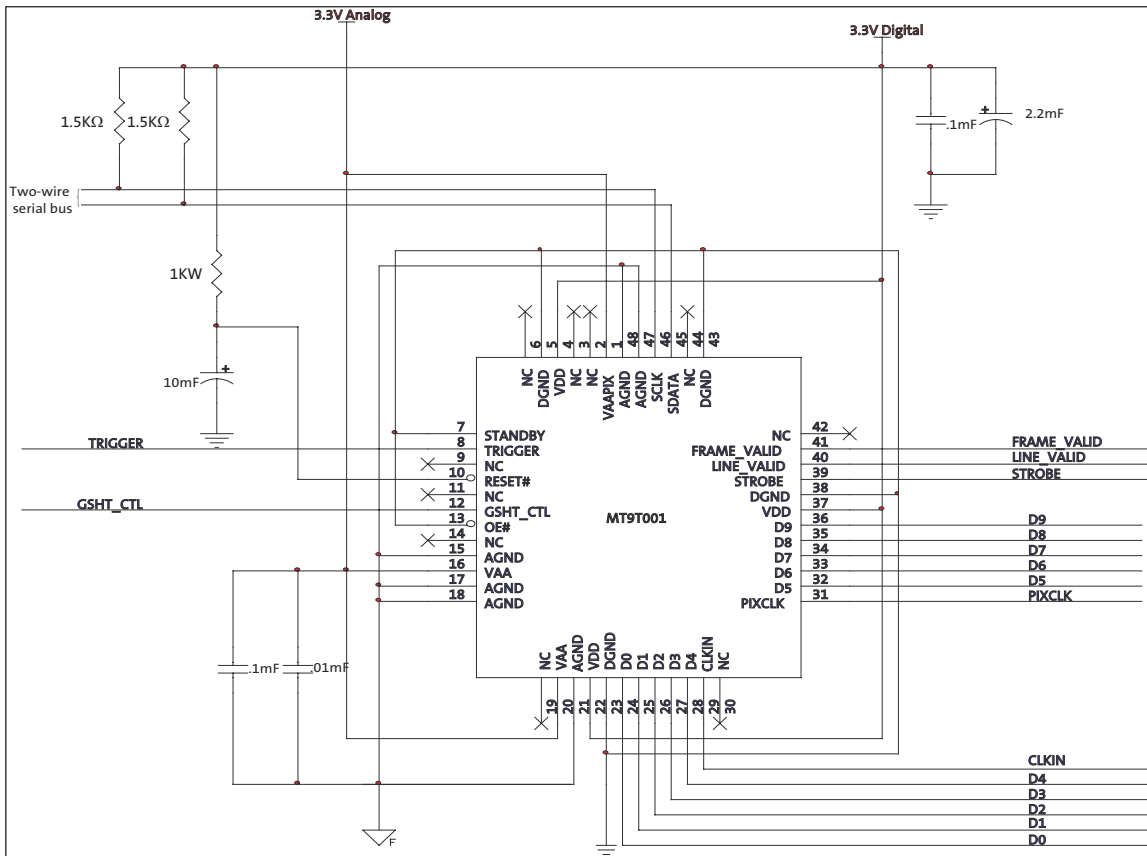


Figure 2: Typical Configuration (Connection)



Note: Resistor value 1.5KΩ is recommended, but may be greater for slower two-wire speed.

Figure 3: 48-Pin PLCC

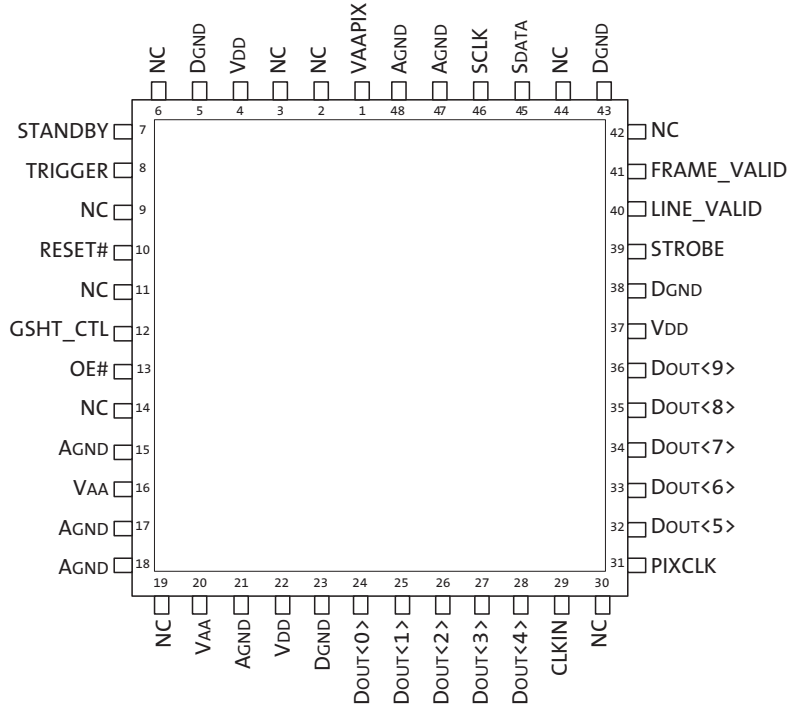


Table 2: Pin Descriptions

Pin Numbers	Symbol	Type	Description
7	STANDBY	Input	Standby: activates (HIGH) standby mode, disables analog bias circuitry for power saving mode.
8	TRIGGER	Input	Trigger: activates (HIGH) snapshot sequence.
10	RESET#	Input	Reset: activates (LOW) asynchronous reset of sensor. All registers assume factory defaults.
13	OE#	Input	Output enable: OE# when HIGH, places outputs DOUT<0–9>, FRAME_VALID, LINE_VALID, PIXCLK, and STROBE into a tri-state configuration.
29	CLKIN	Input	Clock in: master clock into sensor (48 MHz maximum).
46	SCLK	Input	Serial clock: clock for serial interface.
12	GSHT_CTL	Input	Global shutter control.
45	SDATA	I/O	Serial data: serial data bus, requires 1.5K Ω resistor to 3.3V for pull-up.
24, 25, 26, 27, 28, 32, 33, 34, 35, 36	DOUT<0–9>	Output	Data out: pixel data output bit 0, DOUT<9> (MSB), DOUT<0> (LSB).
31	PIXCLK	Output	Pixel clock: pixel data outputs are valid during falling edge of this clock. Frequency = (master clock).
39	STROBE	Output	Strobe: output is pulsed HIGH to indicate sensor reset operation of pixel array has completed.
40	LINE_VALID	Output	Line valid: output is pulsed HIGH during line of selectable valid pixel data (see Reg0x20 for options).
41	FRAME_VALID	Output	Frame valid: output is pulsed HIGH during frame of valid pixel data.

Table 2: Pin Descriptions (continued)

Pin Numbers	Symbol	Type	Description
1	VAAPIX	Supply	Analog pixel power: provide power supply for pixel array, 3.3V ±0.3V.
4, 22, 37	VDD	Supply	Digital power: provide power supply for digital block, 3.3V ±0.3V.
5, 23, 38, 43	DGND	Supply	Digital ground: provide isolated ground for digital block.
16, 20	VAA	Supply	Analog power: provide power supply for analog block, 3.3V ±0.3V.
15, 17, 18, 21, 47, 48	AGND	Supply	Analog ground: provide isolated ground for analog block and pixel array.
2, 3, 6, 9, 11, 14, 19, 30, 42, 44	NC	–	No connect: these pins must be left unconnected.

Pixel Data Format

Pixel Array Structure

The MT9T001 pixel array is configured as 2,112 columns by 1,568 rows, as shown in Figure 4. Columns from 0 through 27 and from 2,085 through 2,111, and also rows from 0 through 15 and from 1,561 through 1,567 are optically black. These optical black columns and rows can be used to monitor the black level. The black row data is used internally for the automatic black level adjustment. However, the black rows and columns can also be read out by setting Reg0x20 (11) and Reg0x1E (7), respectively. There are 2,057 columns by 1,545 rows of optically active pixels, which provides a four-pixel boundary around the QXGA (2,048 x 1,536) image to avoid boundary effects during color interpolation and correction.

The MT9T001 uses a Bayer color pattern, as shown in Figure 5. The even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. The even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels.

Figure 4: Pixel Array Description

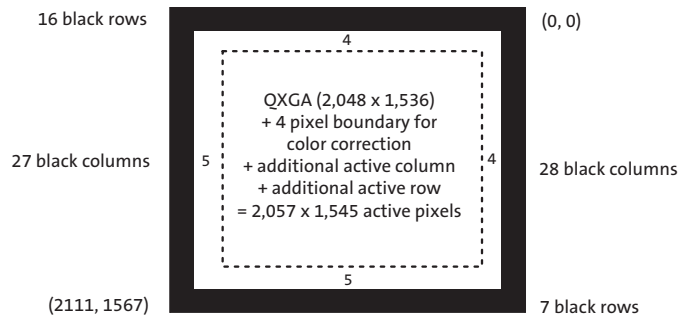
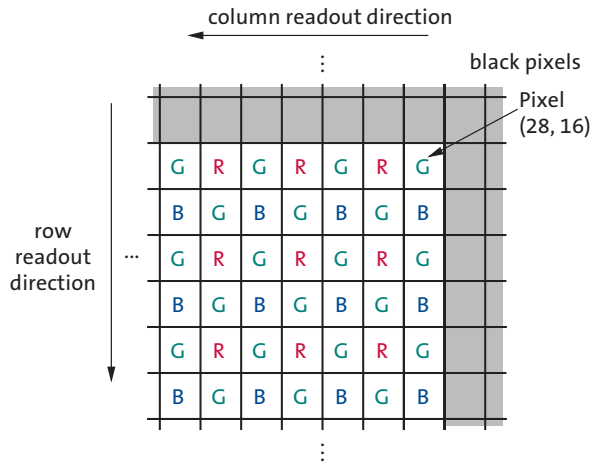


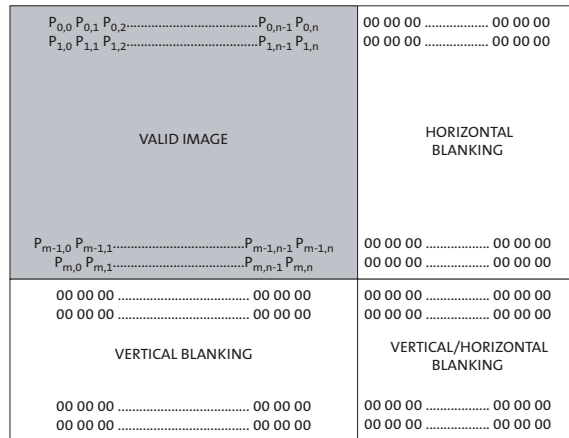
Figure 5: Pixel Color Pattern Detail (Top Right Corner)



Output Data Format

The MT9T001 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 6. The amount of horizontal blanking and vertical blanking is programmable through Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in “Output Data Timing” on page 9.

Figure 6: Spatial Illustration of Image Readout



Output Data Timing

The data output of the MT9T001 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

The PIXCLK can be used as a clock to latch the data. DOUT data is valid on the falling edge of PIXCLK in default mode. The PIXCLK is HIGH while master clock is HIGH and then LOW while master clock is LOW. It is continuously enabled, even during the blanking period. The parameters in P, A, and Q shown in Figure 8 are defined in Table 3.

Figure 7: Timing Example of Pixel Data

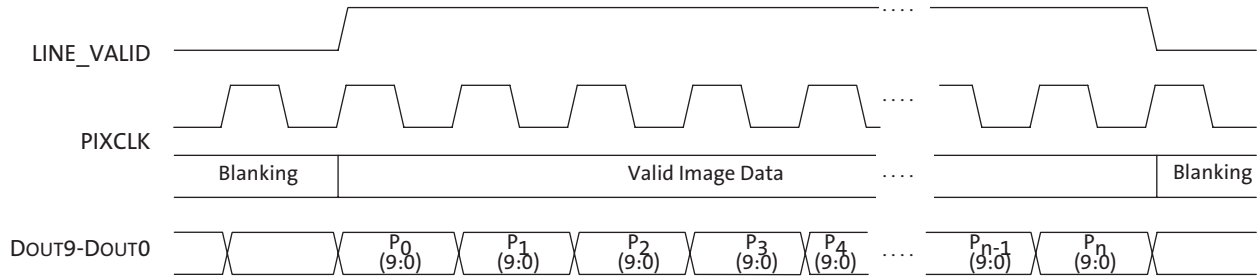
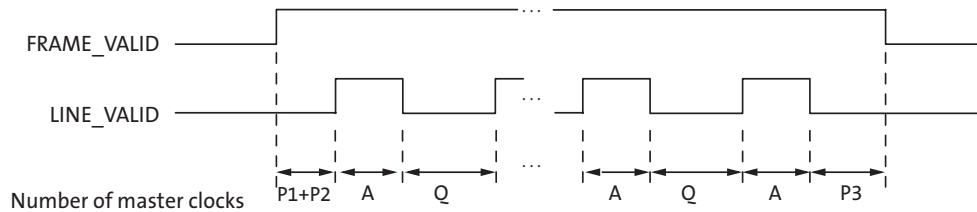


Figure 8: Row Timing and FRAME_VALID/LINE_VALID Signals



Frame Timing Formulas

Table 3: Frame Timing

Parameter	Name	Equation (Pixel Clocks = Master Clock)	Default Timing at 48 MHz
R	Active Rows	$((\text{Reg0x03} + 1) / ((\text{Reg0x22}[2-0] + 1)))$ (rounded up to next even number)	1,536 pixel clocks = 32.0μs
A	Active Columns	$((\text{Reg0x04} + 1) / ((\text{Reg0x23}[2-0] + 1)))$ (rounded up to next even number)	2,048 pixel clocks = 42.67μs
P1	Frame Start Blanking 1	331 if Reg0x22[5-4] = 0, normal 673 if Reg0x22[5-4] = 1, Bin 2x 999 if Reg0x22[5-4] = 2, Bin 3x	331 pixel clocks = 6.89μs
P2	Frame Start Blanking 2	38 if Reg0x23[5-4] = 0, normal 22 if Reg0x23[5-4] = 1, Bin 2x 14 if Reg0x23[5-4] = 2, Bin 3x	38 pixel clocks = 0.79μs
P3	Frame End Blanking 3	Reg0x05 (minimum Reg0x05 value = 21)	142 pixel clocks = 2.96μs
Q	Horizontal Blanking	P1 + P2 + P3	511 pixel clocks = 10.65μs

Table 3: Frame Timing

Parameter	Name	Equation (Pixel Clocks = Master Clock)	Default Timing at 48 MHz
P4	Shutter Overhead	$\text{Reg0x0C} + 316 \times (\text{Reg0x23}[5-4] + 1)$	316 pixel clocks = 6.58 μ s
t_{ROW}	RowTime	The greater of: (A + Q) or (P1+ P4)	2,559 pixel clocks = 53.31 μ s
V	Vertical Blanking	$(\text{Reg0x06} + 1) \times t_{\text{ROW}}$	66,534 pixel clocks = 1.39ms
t_{FV}	Frame Valid Time	$R \times t_{\text{ROW}}$	3,930,624 pixel clocks = 81.89ms
t_{FRAME}	Total Frame Time	The greater of: $((65536 \times \text{Reg0x08} + \text{Reg0x09}) \times t_{\text{ROW}})$ or $(t_{\text{FV}} + V)$	3,997,158 pixel clocks = 83.27ms

Feature Description

Window Control

- **Reg0x01, Reg0x02, Reg0x03, and Reg0x04**

These registers control the size of the window.

Window Size

The default programmed window size is 2,048 columns by 1,536 rows (2,048H x 1,536V). The control logic allows the flexibility to change the window size by programming Reg0x03 and Reg0x04. Reg0x03 controls the window height (number of rows) and Reg0x04 controls the window width (number of columns). The value to be programmed in Reg0x03 is the desired number of rows - 1. The value to be programmed in Reg0x04 is the desired number of columns - 1.

The minimum value for Reg0x03 is 0x0001; for Reg0x04, 0x0001. Thus, the smallest window size is two columns by two rows (2H x 2V). The value of Reg0x03 and Reg0x04 must be an odd number (there can only be even number of columns). The user can program the window size to be any format desired. Table 4 shows examples of register settings to achieve various resolutions and frame rates.

Table 4: Standard Resolutions

Resolution	Frame Rate	Column_Size (Reg0x04)	Row_Size (Reg0x03)	Shutter Width (Reg0x09)
2,048 x 1,536 QXGA	12 fps	2,047	1,535	<1,552
1,600 x 1,200 UXGA	20 fps	1,599	1,199	<1,216
1,280 x 1,024 SXGA	27 fps	1,279	1,023	<1,040
1,024 x 768 XGA	43 fps	1,023	767	<784
800 x 600 SVGA	65 fps	799	599	<616
640 x 480 VGA	93 fps	639	479	<496

Table 5: Wide Screen (16:9) Resolutions

Resolution	Frame Rate	Column_Size (Reg0x04)	Row_Size (Reg0x03)	Shutter Width (Reg0x09)
1,920 x 1,080 HDTV	18 fps	1,919	1,079	<1,096
1,280 x 720 HDTV	39 fps	1,279	719	<736

Note: For Table 4 and Table 5 above, the settings for Reg0x05 (horizontal blanking) and Reg0x06 (vertical blanking) are 21 and 15 respectively, while all of the registers are set to default.

Electronic Panning

In addition to changing the window size, the user has the flexibility to change the location of the readout window. Reg0x01 controls the first row to be read out and Reg0x02 controls the first column to be read out. The default values are 0x0014 (decimal 20) for Reg0x01 and 0x0020 (decimal 32) for Reg0x02. The first column to be read out must be an even number.

Reg0x01 and Reg0x02, together with Reg0x03 and Reg0x04, allow the user to choose any segment of the imager array to be read out. This is especially beneficial when the user needs to zoom in on a small portion of the image and perform analysis on the image content.

Figure 9 shows some examples of the electronic panning/zoom-in and windowing capabilities of the sensor.

Blanking Control

Reg0x05 and Reg0x06

These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. The actual imager timing can be calculated using the equations given in Table 3 on page 10.

Reg0x05 controls the horizontal blanking time in a row. The value is specified in terms of pixel clocks. Default value of 0x008E for Reg0x05 results in a horizontal blanking time of 511 pixel clocks. The minimum value for Reg0x05 is 21. Thus, the minimum horizontal blanking time is 390 pixel clocks.

Reg0x06 controls the vertical blanking time in a row. The value is specified in terms of the number of rows. Default value of 0x0019 for Reg0x06 results in a vertical blanking time of 26-row time.

Frame Time

Reg0x03, Reg0x04, Reg0x05, and Reg0x06

Total frame time in terms of pixel clocks can be obtained using the formula given in Table 3 on page 10. The user can change the number of columns and rows read out, horizontal blanking and vertical blanking times to obtain different frame rates.

High Frame Rate Readout Modes

Reg0x01, Reg0x02, Reg0x03, Reg0x04, Reg0x05, and Reg0x06

In addition to having the flexibility to read out smaller standard formats, the sensor gives the user the option of reading out nonstandard formats. This is particularly useful if the user needs to zoom in on a particular segment of the image to perform high-speed mathematical calculations (e.g., high-speed viewfinder or auto focus applications).

In applications such as the auto focus mode, the user may need more horizontal resolution than vertical. Thus, the user can window down to the mid-section of the imager array by programming Reg0x01 and Reg0x03 to change the row start address and the window height. Figure 10 is an example of how the user may want to window down to 2,048H x 512V from the default of 2,048H x 1,536V. See also Table 6 for other auto focus mode resolutions.

Figure 9: Windowing Capabilities

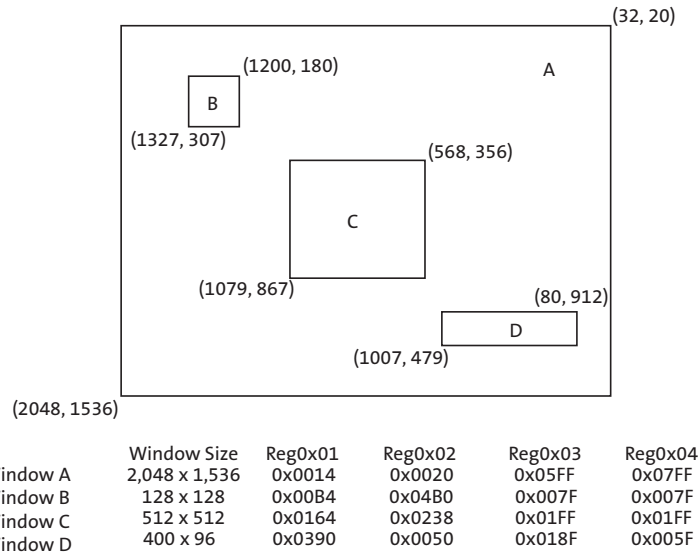
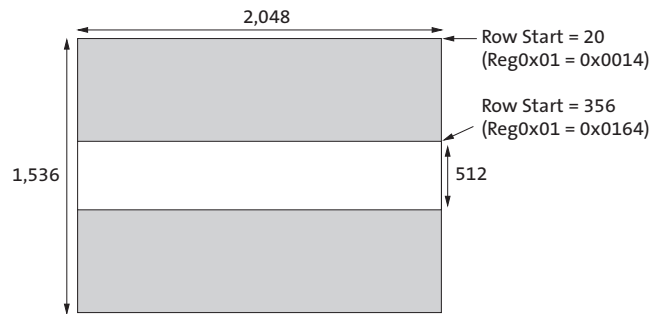


Table 6: Auto Focus Modes

Resolution	Frame Rate	Column Size (reg0x04)	Row Size (reg 0x03)	Horizontal_Bla nk (reg0x05)	Vertical_Blan k (reg0x06)	Row (reg 0x22)	Row_Skip (reg 0x22)	Column_Bin (reg0x23)	Column_Skip (reg0x23)
2,048 x 512	30 fps	2,047	1,535	22	1	2	2	0	0
2,048 x 256	60 fps	2,047	1,535	22	0	2	5	0	0
2,048 x 128	120 fps	2,047	1,023	34	14	1	7	0	0

Figure 10: Windowing



The user can change Reg0x05 and Reg0x06 to obtain the desired frame rate. Also, the user may want to perform row skip modes to obtain larger field of view if high-frequency vertical resolution is not critical.

Pixel Integration Time Control

Reg0x09 and Reg0x0C

The integration time of the pixel is the amount of time the pixels are set to collect charge generated from light. The user can change the integration time of the sensor by programming Reg0x09. The value of Reg0x09 sets the number of row time for integration. The sensor also supports sub-row integration time for fine control of pixel integration time.

The formula for calculating the pixel integration time is (reference Table 3 on page 10 for P1 description):

$$t_{INT} = (65536 \times \text{Reg0x08} + \text{Reg0x09}) \times t_{ROW} - \text{Reg0x0C} - P1 + 132$$

Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. However, if Reg0x09 is increased beyond the total number of rows per frame, then additional blanking rows are added as needed.

While the user can adjust the integration time to the desired value according to the aforementioned formula, not all integration times may be desired under certain lighting conditions. If the light source has a flicker component, then the integration time needs to be set properly to avoid banding in the image.

Under 60Hz flicker, the integration time must be a multiple of 1/120 of a second to avoid flicker. Under 50Hz flicker, the integration time must be a multiple of 1/100 of a second to avoid flicker.

Snapshot Mode and Flash Control

Reg0x1E, STROBE pin and TRIGGER pin

Setting up for Snapshot Mode

Snapshot mode must be enabled before use by setting bit 8 = "1" of Reg0x1E. There are two important signals used for snapshot mode: TRIGGER and STROBE. The TRIGGER signal initiates the start of a single frame capture and STROBE is an output pulse that may be used to turn on a flash and/or activate a mechanical shutter.

Triggering A Snapshot

The TRIGGER signal required for starting a frame capture may be generated in the following two ways:

1. External TRIGGER Pulse
Pin 8 is a digital input that may be used to supply an external trigger signal input. The snapshot operation begins after the TRIGGER pulse transitions from a HIGH to LOW state.
2. TRIGGER from Register Setting
A second method for triggering a snapshot is by setting bit 0 = 1 of Reg0x0B (Restart). This register automatically returns bit 0 to "0" after the TRIGGER is initiated. This bit does not need to be reset by the user after use.

Strobe Pulse Output

The STROBE pulse must be enabled before use by setting Reg0x1E [bit 9] = 1. The STROBE signal has two options for pulse length and may be selected using Reg0x1E [bit 10] as shown in Table 7.

Table 7: STROBE Pulse Output

Reg0x1E, Bit 10	STROBE Pulse Width
0	1 row time (default)
1	$((655326 \times \text{Reg0x08} + \text{Reg0x09} - R) - 16) \times {}^t\text{ROW} - V$

After the TRIGGER pulse has signaled a snapshot operation, each row of the imager array is reset in sequence to clear out any accumulated signal. Once each row of the imager is reset, the STROBE pulse is output from the imager with a length dependent upon the characteristics described above. After the STROBE pulse goes low, the imager waits 16 additional rows and then each row from the pixel array is read out. No STROBE is generated unless the shutter width is greater than the output image height plus vertical blanking.

Global Shutter Release Snapshot Mode

Reg0x1E and Reg0x21

In addition to the standard snapshot mode, the MT9T001 has a global shutter release mode which may be combined with a mechanical shutter to achieve simultaneous exposure of all rows in the image.

Two global shutter modes are available: programmed exposure and bulb mode. In programmed exposure mode, the exposure time is dictated by {Reg0x08, Reg0x09} (Shutter Width). In bulb mode, the TRIGGER and GSHT_CTL pins are used to achieve an arbitrary exposure time.

Programmed Exposure Mode

To use programmed exposure mode:

1. Set up snapshot mode as normal (including any STROBE preferences).
2. Set Reg0x21 (Read Mode 3) to 0x0003.
3. Assert (transition LOW to HIGH) the GSHT_CTL pin to reset the array. This pin must remain HIGH for 18820 PIXCLKs.
4. Negate (transition HIGH to LOW) the GSHT_CTL pin to begin the exposure. The exposure starts 1000 PIXCLKs after the falling edge of GSHT_CTL.

Note: Unlike normal snapshot mode, Reg0x0B (Restart) may not be used to initiate the exposure in global shutter modes.

5. Row readout begins automatically. The mechanical shutter should be closed before row read out begins. The trailing edge of STROBE (if enabled) occurs $((65536 \times \text{Reg0x08} + \text{Reg0x09}) \times {}^t\text{ROW} + 2000)$ PIXCLKs after the falling edge of GSHT_CTL. Readout of the active window starts the lesser of $16 \times {}^t\text{ROW}$ or $(\text{Reg0x06} + 1) \times {}^t\text{ROW}$ later.

Bulb Mode

To use bulb mode:

1. Set up snapshot mode as normal (including any STROBE preferences).
2. Set Reg0x21 (Read Mode 3) to 0x0001.
3. Assert (transition LOW to HIGH) the GSHT_CTL pin.

4. Assert (transition LOW to HIGH) the TRIGGER pin to reset the array. This pin must remain HIGH for at least 18,820 PIXCLKs.
5. Negate (transition HIGH to LOW) the GSHT_CTL pin to begin the exposure. The exposure starts 1,000 PIXCLKs after the falling edge of GSHT_CTL.

Note: Unlike normal snapshot mode, Reg0x0B (Restart) may not be used to initiate the exposure in global shutter modes.

6. Negate (transition HIGH to LOW) the TRIGGER pin to begin row read out. The mechanical shutter should be closed before row read out begins. The trailing edge of STROBE (if enabled) occurs $((65536 \times \text{Reg0x08} + \text{Reg0x09}) \times \text{ROW})$ PIXCLKs after the falling edge of TRIGGER. Read out of the active window starts the lesser of $16 \times \text{ROW}$ or $(\text{Reg0x06} + 1) \times \text{ROW}$ later. In this mode, the shutter width (Reg0x08, Reg0x09) would normally be set to a low number, allowing row readout to start immediately after the trailing edge of TRIGGER.

Skip and Bin Modes

Row and column skip modes use subsampling to reduce the output resolution without reducing field-of-view. The MT9T001 also has row and column binning modes, which can reduce the impact of aliasing introduced by the use of skip modes. This is achieved by the averaging of two or three adjacent rows and columns (adjacent same-color pixels). Both 2x and 3x binning modes are supported. Rows and columns can be binned independently.

Table 8: Bin and Skip Mode Resolution

Resolution	Frame Rate	Column Size (reg0x04)	Row Size (reg 0x03)	Horizontal Blank (reg0x05)	Vertical Blank (reg0x06)	Row Bin (reg 0x22)	Row Skip (reg 0x22)	Column Bin (reg0x23)	Column Skip (reg0x23)
1,024 x 768 XGA	34 fps	2,047	1,535	22	40	1	1	1	1
800 x 600 SVGA	50 fps	1,599	1,199	22	30	1	1	1	1
640 x 480 VGA	48 fps	1,919	1,439	21	31	2	2	2	2

Note: Column start address value must be a multiple of Reg0x23 [5–4] + 1.

To use binning mode, set Reg0x22[5–4] (row bin) or Reg0x23[5–4] (column bin) to the desired reduction minus 1, as would be done for skip mode. Additionally, Reg0x22[2–0] (column skip) must be set no less than Reg0x22[5–4], and Reg0x23[2–0] (row skip) must be set no less than Reg0x23[5–4]. Row and column skip modes may be set higher than the corresponding binning modes to achieve greater reductions, but binning must be done. The different skip modes supported are between 2x and 8x in both column and row directions. The different binning modes supported are 2x and 3x. See Table 9 for register bits controlling the different bin and skip modes.

Table 9: Skip and Bin Modes

Register Bit	Skip/Bin Modes	Readouts
Reg0x23 Bit[2-0]	No column skip Column skip 2x Column skip 3x Column skip 4x Column skip 8x	col0, col1, col2, col3, col4, col5, etc. col0, col1, col4, col5, col8, col9, etc. col0, col1, col16, col7, col12, col13 etc. col0, col1, col8, col9, col16, col17, etc. col0, col1, col16, col17, col32, col33, etc.
Bit[5-4]	Column Bin 2x Column Bin 3x	Binning of 2 adjacent same-color pixels in a 4x4 window Binning of 3 pixel of each color plane in a 6x6 window
Reg0x22 Bit[2-0]	No row skip Row skip 2x Row skip 3x Row skip 4x Row skip 8x	row0, row1, row2, row3, row4, row5, etc. row0, row1, row4, row5, row8, row9, etc. row0, row1, row6, row7, row12, row13, etc. row0, row1, row8, row9, row16, row17, etc. row0, row1, row16, row17, row32, row33, etc.
Bit[5-4]	Row bin 2x Row bin 3x	Binning of 2 pixel of each color plane in a 4x4 window Binning of 3 pixel of each color plane in a 6x6 window

Note: Column and row skip modes 1x through 8x are available on the MT9T001. Also, the read outs shown assume column start and row start addresses are both "0".

Figure 11: Column Skip 2x; Row Skip 2X Enabled

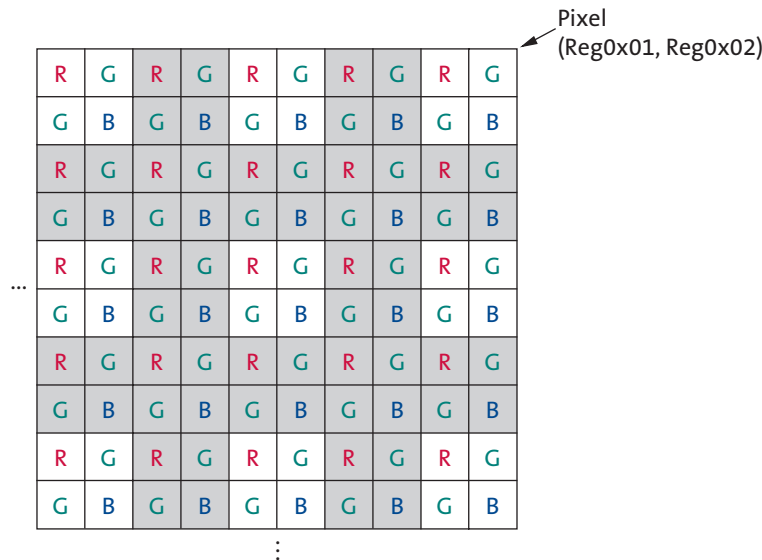


Figure 12: Column Skip 3x; Row Skip 3X Enabled

R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B

Pixel (Reg0x01, Reg0x02)

Figure 13: Column Skip 4x; Row Skip 4X Enabled

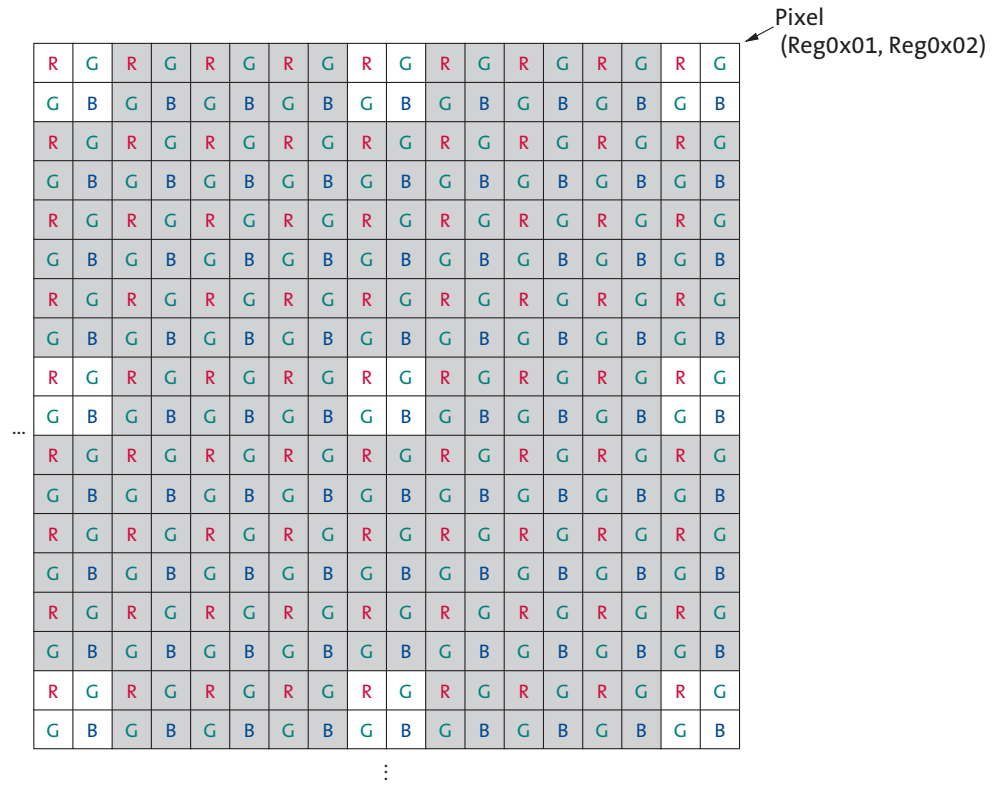


Figure 14: Column Skip 8x; Row Skip 8X Enabled

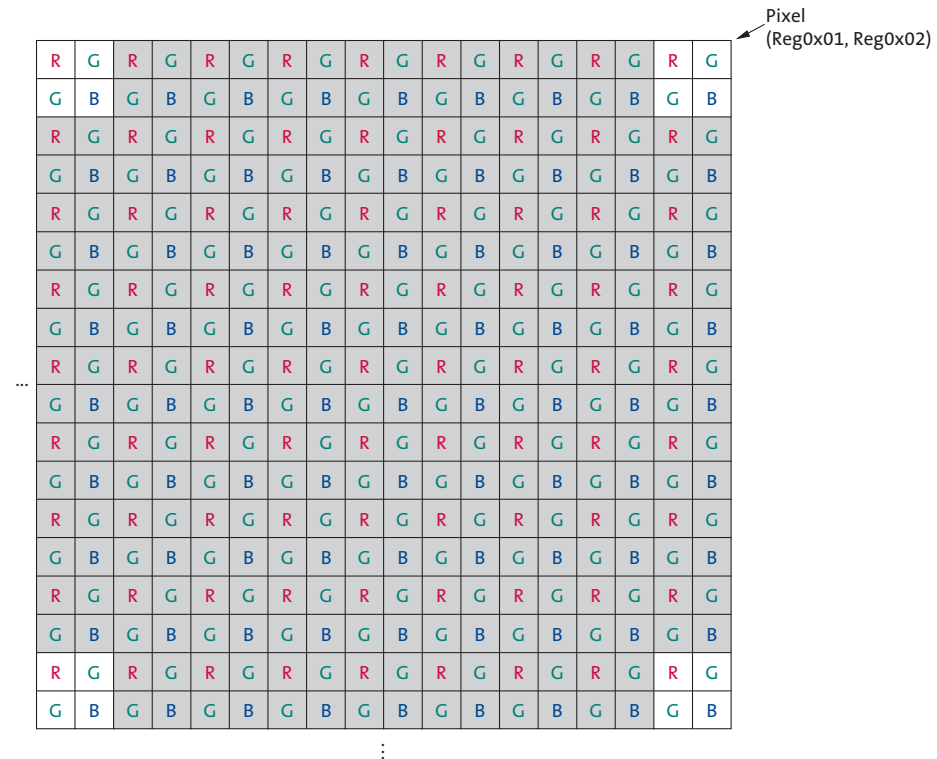


Figure 15: Bin 2-to-1: 2,048H x 1,536V (QXGA) to 1,024H x 768V (XGA)

Note: Grs = binning of 4 Gr[s] in a 4 x 4 window; Gbs = binning of 4 Gb[s] in a 4 x 4 window.
Rs = binning of 4 R[s] in a 4 x 4 window; Bs[s] = binning of 4 B[s] in a 4 x 4 window.

Figure 16: Bin 3-to-1: 2,048H x 1,536V (QXGA) to 640H x 480V (VGA)

Note: Grs = binning of 9 Gr[s] in a 6 x 6 window; Gbs = binning of 9 Gb[s] in a 6 x 6 window.
Rs = binning of 9 R[s] in a 6 x 6 window; Bs = binning of B[s] in a 6 x 6 window.

Smaller Format Resolution

Reg0x01, Reg0x02, Reg0x03, Reg0x04, Reg0x05, Reg0x06, Reg0x22, and Reg0x23

With the aforementioned flexible windowing capability of the sensor, the user is able to read out different resolution formats from default of QXGA to UXGA, SXGA, XGA, SVGA, VGA, CIF, QVGA, QCIF, etc. Below are some examples of programmable register settings to obtain the estimated frame rates for the desired formats.

The user can change the values of Reg0x05 and Reg0x06 to obtain different frame rates. The field of view of the image is reduced since the programmed settings effectively reduce the read out window to the specified settings without skipping any rows or columns.

If the user only changes the register settings mentioned above without changing the row and column start address, the read out window would start from that coordinate. To read out the center of the image or any portion that is desired, the user would need to program Reg0x01 and Reg0x02, thus performing electronic panning.

To maintain the same field of view while reducing the read out resolution, the user would need to perform row and column skip. For example, if the desired read out resolution needs to be XGA (1,024H x 7,68V) instead of QXGA (2,048H x 1,536V). To maintain the same field of view, the user can select column skip 2x and row skip 2x modes. This

effectively reduces the horizontal and vertical resolution by 2x for a factor of 4x reduction in overall number of pixels that are read out. To perform this read out mode, the user would need to set the following:

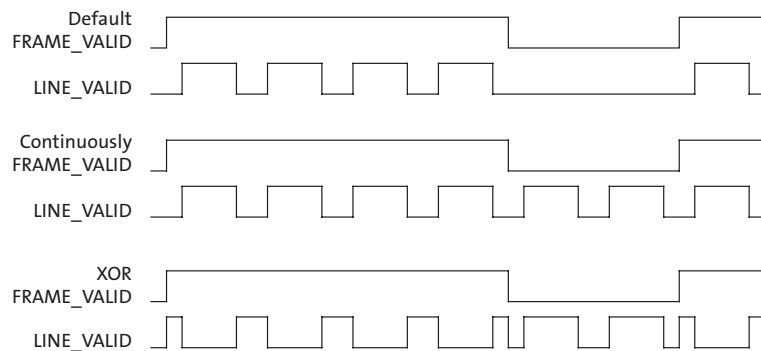
Reg0x03 =	1,536V rows
0x05FF	
Reg0x04 =	2,048H columns
0x07FF	
Reg0x23	Column skip 2x—> 1,024H
Bit[2:0]=1	columns read out
Reg0x22 Bit[2:0]	Row skip 2x —> 768
= 1	rows read out

If the user sets Reg0x03 = 0x02FF (768V rows), Reg0x04 = 0x03FF (1,024H columns), and then enable column skip 2x and row skip 2x, the effective readout resolution is 512H x 384V.

Line_Valid Formats

Reg0x20 is used to control many aspects of the readout of the sensor. By setting Bit 9 and 10 of Reg0x20 the LINE_VALID signal can get three different output formats. The formats are shown in Figure 17 when reading out four rows and two vertical blanking rows. In the last format the LINE_VALID signal is the XOR between the continuously LINE_VALID signal and the FRAME_VALID signal.

Figure 17: Different LINE_VALID Formats



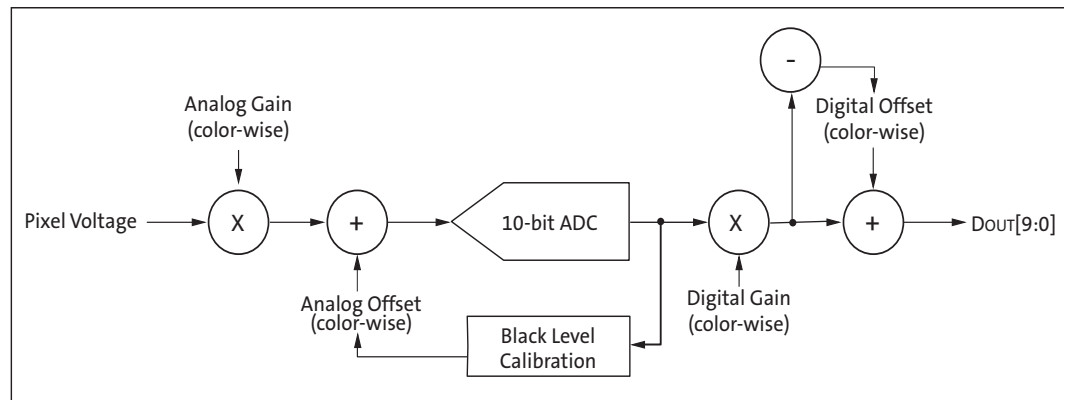
Signal Path

The MT9T001 sensor analog signal path consists of the pixel array, the column sample and hold (S/H) circuitry, the programmable gain stage, the analog offset correction and the analog-to-digital converter (ADC).

The reset and signal voltages from the pixel are sampled onto the column sample and hold circuitry on a row-wise basis. After signal sampling is complete, the differential signal (reset – signal) is transferred to the programmable gain stage.

After the gain stage, the differential signal goes through the analog offset correction circuitry. The user can decide if a positive or negative offset or no offset needs to be added to the differential signal. The signal is then sampled onto the sample and hold circuitry of the ADC before being digitized.

Figure 18: Signal Path



Gain Settings

Reg0x2B, Reg0x2C, Reg0x2D, Reg0x2E, and Reg0x35

The analog programmable gain stage consists of two stages of gain circuitry that operate in a pipelined manner. The first stage of gain has programmable gain of 1 or 2 while the second stage of gain has programmable gain of 1 to 4 with steps of 0.125 for a maximum analog gain of 8. The gain settings can be independently adjusted for the colors of Green1, Blue, Red, and Green2 and are programmed through Reg0x2B, Reg0x2C, Reg0x2D, and Reg0x2E, respectively. The gain may also be adjusted globally through Reg0x35. The first stage of gain is set by Bit(6), while the second stage gain is set by Bit(5–0). The gain is individually controllable for each color in the Bayer pattern as follows:

Analog Gain ≤ 8 :

$$\text{Gain} = (\text{Bit}[6] + 1) \times (\text{Bit}[5:0] \times 0.125)$$

$$\text{Digital Gain} = 1 + \text{Bit}[14:8]/8$$

$$\text{Total Gain} = \text{Analog Gain} \times \text{Digital Gain}$$

Since Bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain, as shown in Table 10.

Table 10: Gain Increment Settings

Nominal Gain	Increments	Recommended Settings
1 to 4.000	0.125	0x0008 to 0x0020
4.25 to 8.00	0.25	0x0051 to 0x0060
9.0 to 128.0	1.0	0x0160 to 0x7860

Black Level Calibration

Reg0x5D, and Reg0x5F

The digitized black level of the MT9T001 sensor potentially varies with temperature or gain setting changes. The MT9T001 sensor allows the user the flexibility of automatic black level calibration or manual black level control.

Manual Black Level Calibration

Reg0x60, Reg0x61, Reg0x62, Reg0x63, and Reg0x64

The programmable analog offset stage corrects for analog offset that might be present in the analog signal. The user would need to program Reg0x62 appropriately to enable the analog offset correction. The analog offset settings can be independently adjusted for the colors of Green1, Green2, Red and Blue and are programmed through Reg0x60, Reg0x61, Reg0x63 and Reg0x64 respectively. Bit[8] of Reg0x60, Reg0x61, Reg0x63 and Reg0x64 (these registers have two's complement representation) determines the sign of the analog offset. Bit[8] = 1 makes the analog correction negative instead of positive.

The lower 8 bits (Bit[7:0]) determine the absolute value of the analog offset to be corrected and Bit[8] determines the sign of the correction. When Bit[8] is "1", the sign of the correction is negative and vice versa. The analog value of the correction relative to the analog gain stage can be determined from the following formula:

$$\text{Analog offset} = \text{Bit}[8:0] \times 1 \text{ LSB}$$

The 1 LSB value in the formula is an estimate amount. It deviates from 1 LSB with process variation.

Black Level

Reg0x49

Digital offset is applied such that the average black level of a frame in a resulting image equals the value of this register. This adjustment happens after black level calibration.

Reset

This register is used to reset the sensor registers to their default, power-up state. To reset the MT9T001, first write a "1" into bit 0 of this register to put the MT9T001 in reset mode, then write a "0" into bit 0 to resume operation.

Another way to reset the sensor is through the RESET# (pin 10) – by pulling the RESET# signal to 0V.

The reset operation is an asynchronous reset and the sensor remains in reset as long as RESET# signal = 0V. In both methods of reset, the sensor register settings returns to their default states.

Standby Control and Chip Enable

There are two steps required to put the sensor in standby mode:

1. Through the two-wire serial interface program Reg0x07 Bit[1] = 0. This stops the sensor readout and powers down analog circuitry of the sensor. The sensor stays in standby mode until the user reprograms Reg0x07 Bit[1] = 1.
2. Set STANDBY (pin 7) to HIGH.

Serial Bus Description

Registers are written to and read from the MT9T001 through the two-wire serial interface bus. The MT9T001 is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9T001 through the serial data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5K Ω resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- a(n) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request is a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9T001 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the

register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The eight-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A “0” (0xBA) in the LSB (least significant bit) of the address indicates write mode, and a “1” (0xBB) indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

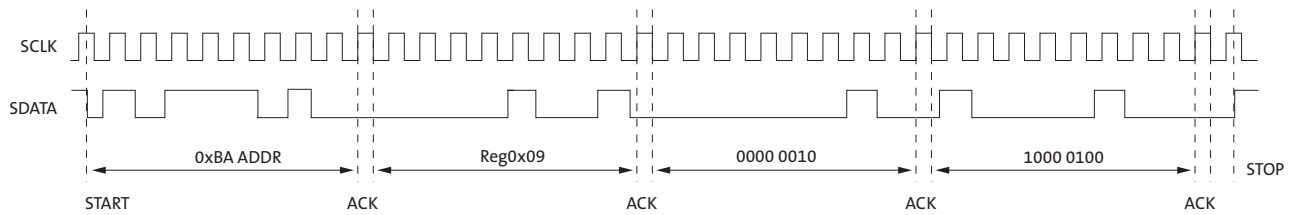
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 19. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then gives an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit transfer, the image sensor gives an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

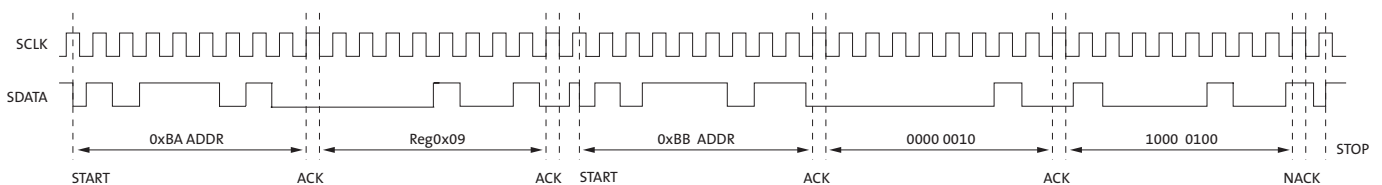
Figure 19: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 20. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 20: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284



Electrical Specifications

Data Output and Propagation Delays

By default, the MT9T001 launches pixel data, FRAME_VALID and LINE_VALID with the rising edge of PIXCLK. The expectation is that the user captures DOUT[9:0], FRAME_VALID and LINE_VALID using the rising edge of PIXCLK.

Figure 21: Data Output Timing Diagram

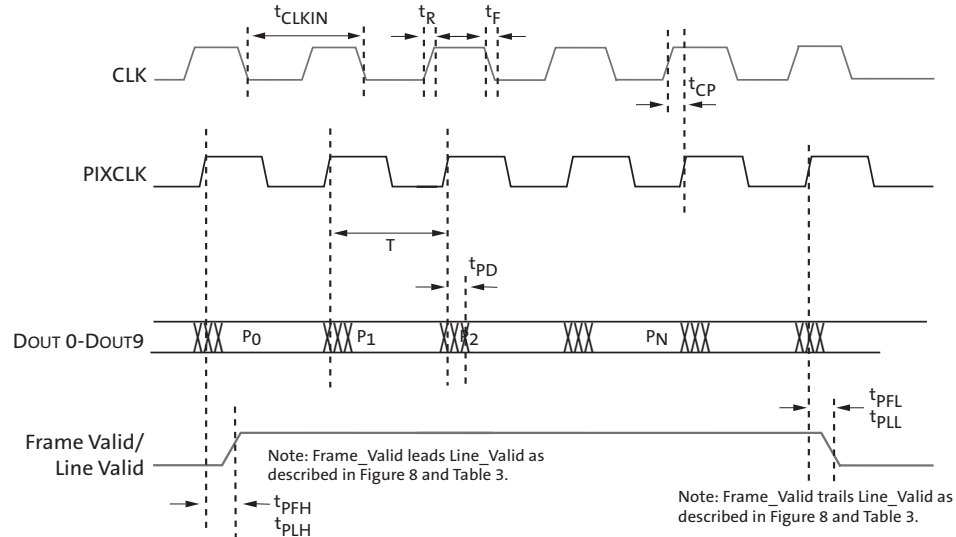


Table 11: DC Electrical Characteristics

(DC Setup Conditions: $f_{CLKIN} = 48 \text{ MHz}$, $V_{DD} = 3.3\text{V}$, $V_{AA} = 3.3\text{V}$, $V_{AAPIX} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$)

Symbol	Definition	Condition	Min	Typ	Max	Units
VDD	Core digital voltage		3	3.3	3.6	V
VAA	Analog voltage		3	3.3	3.6	V
VAAPIX	Pixel supply voltage		3	3.3	3.6	V
VIH	Input high voltage		1.70			V
VIL	Input low voltage				1.45	V
IIN	Input leakage current	No Pull-up Resistor; $V_{IN} = V_{DD}$ or DGND	-5		5	μA
VOH	Output high voltage	At specified IOH	3.3			V
VOL	Output low voltage	At specified IOL	0		0.3	V
IOH	Output high current	At specified VOH			11.5	mA
IOL	Output low current	At specified VOL			12.5	mA
IOZ	Tri-state output leakage current				5	μA
IDD	Digital operating current	0 lux, 48 MHz		20	23.0	mA
IAA	Analog operating current	0 lux, 48 MHz		45.0	54.0	mA
IAAPIX	Pixel supply current	0 lux, 48 MHz		4.0	5.0	mA
ISTDBYD	Digital standby current	Input clock disabled, 0 lux		0.2	2.0	μA
ISTDBYA	Analog standby current	Input clock disabled, 0 lux		0.2	2.0	μA
ISTDBYDA	Pixel standby current	Input clock disabled, 0 lux		0.1	1.0	μA

Table 12: AC Electrical Characteristics

(AC Setup Conditions: $f_{CLKIN} = 48 \text{ MHz}$, $V_{DD} = 3.3\text{V}$, $V_{AA} = 3.3\text{V}$, $V_{AAPIX} = 3.3\text{V}$, V_{DDPLL} , $T_A = 25^\circ\text{C}$)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{CLKIN}	Input clock frequency		1		48	MHz
t_{CLKIN}	Input clock period		1000		20.8	ns
T	PIXCLK period		1000		20.8	ns
t_R	Input clock rise time			4		V/ns
t_F	Input clock fall time			4		V/ns
	Clock duty cycle		45		55	%
t_{CP}	CLKIN to PIXCLK propagation delay			5	2	ns
t_{PD}	PIXCLK to data valid				2	ns
t_{PFH}	PIXCLK to FRAME_VALID HIGH	Default			2	ns
t_{PLH}	PIXCLK to LINE_VALID HIGH	Default			2	ns
t_{PFL}	PIXCLK to FRAME_VALID LOW	Default			2	ns
t_{PLL}	PIXCLK to LINE_VALID LOW	Default			2	ns
CLOAD	Load capacitance				30	pF

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
		Min	Max	
T_{OP}	Operating temperature	0	60	$^\circ\text{C}$
T_{ST}^1	Storage temperature	-40	125	$^\circ\text{C}$

Note: ¹Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 22: Serial Host Interface Start Condition Timing

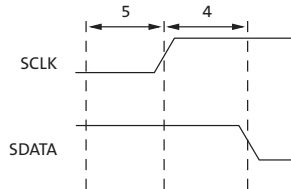
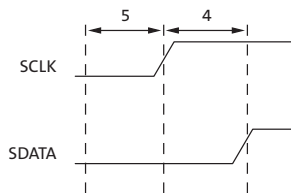
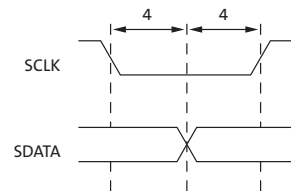


Figure 23: Serial Host Interface Stop Condition Timing



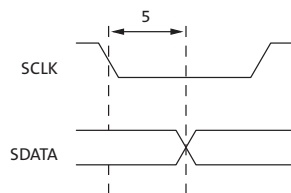
Note: All timing are in units of master clock cycle.

Figure 24: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 25: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 26: Acknowledge Signal Timing After an 8-Bit Write to the Sensor

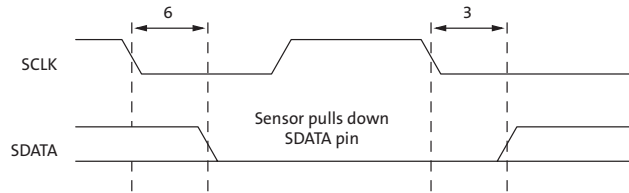
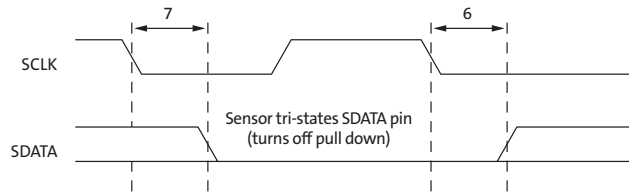
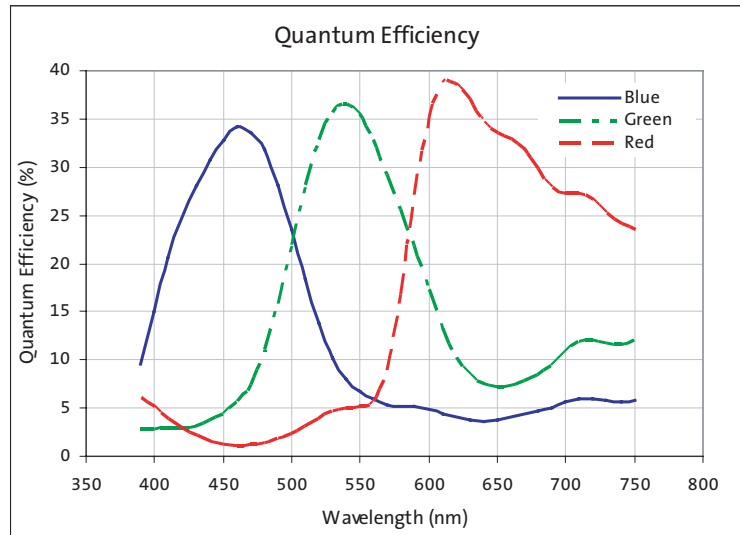


Figure 27: Acknowledge Signal Timing After an 8-Bit Read from the Sensor



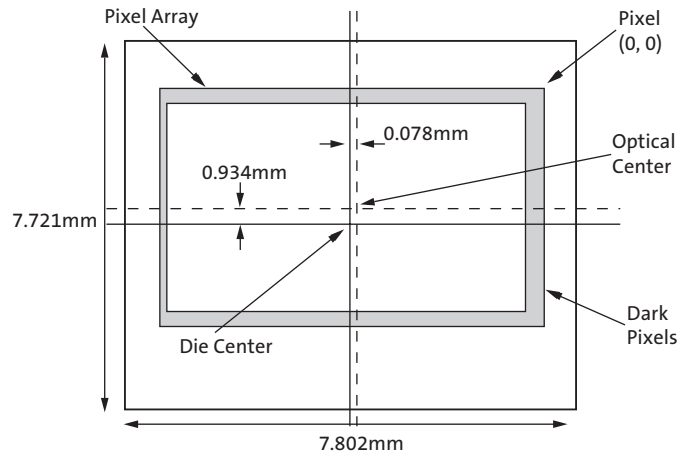
Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Figure 28: Quantum Efficiency



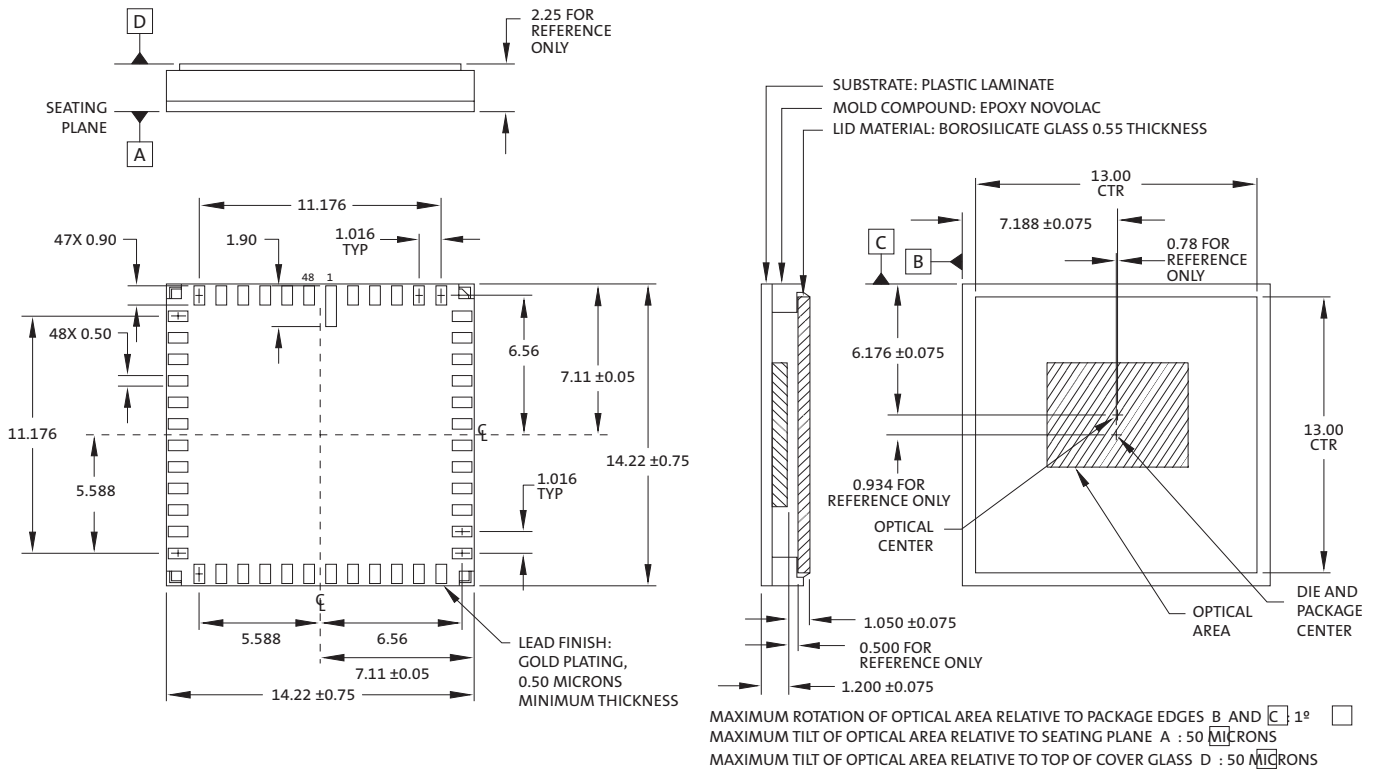
Note: Diagram not to scale.

Figure 29: Image Center Offset



Note: Diagram not to scale.

Figure 30: 48-Pin PLCC



Note: All dimensions in millimeters.

Revision History

Rev. G		5/3/11
	<ul style="list-style-type: none"> • Updated trademarks • Applied updated template 	
Rev. F		6/10
	<ul style="list-style-type: none"> • Updated to non-confidential 	
Rev E.....		5/10
	<ul style="list-style-type: none"> • Updated to Aptina template 	
Rev D		07/05
	<ul style="list-style-type: none"> • Remove Preliminary designation • Updated Table 1, “Key Performance Parameters,” on page 1 • Updated Table 3, “Register List and Default Values,” on page 8 • Updated Table 4, “Reserved Register List and Default Values,” on page 9 • Updated Table 5, “Register Descriptions,” on page 11 • Updated Table 11, “DC Electrical Characteristics,” on page 28 • Updated Table 12, “AC Electrical Characteristics,” on page 29 • Add Table 13, “Absolute Maximum Ratings,” on page 29, and NOTE • Updated page 33 (text, Figure 21 replaced, Figure 22 deleted) • Added Figure 28, Quantum Efficiency, on page 31 • Removed Die Placement figure • Updated Figure 30, 48-Pin PLCC, on page 33 	
Rev C, Preliminary		09/04
	<ul style="list-style-type: none"> • Added Applications • Updated Image Center Offset, Figure 30 	
Rev B, Preliminary		03/04
	<ul style="list-style-type: none"> • Updated Figure 29 • Added Table 1, Key Performance Parameters, on page 1 • Updated Tables 2, 4, 5 and 6 	
Rev A.....		12/03
	<ul style="list-style-type: none"> • Initial Release of document 	